1. Mikroişlemcili Sistem Tasarımına Giriş

Y.Doç. Dr. Tuncay UZUN, 3 Ekim 2005

Dersin Kodu: 140 4150
Dersin Kredisi: 3
Ders Süresi: 3 saat Teori

Dersin Amacı :

Günümüzde, ticari, endüstriyel, tıbbi, askeri vs. uygulamalarda yaygın olarak kullanılan IBM uyumlu kişisel bilgisayar türevlerinde merkezi işlem birimi olarak bulunan 80x86 temelli gelişmiş mikroişlemcilere sahip sistemlerin ve çevre birimlerinin donanım ve yazılım özelliklerinin incelenmesi, tasarlanması ve uygulamasının öğretilmesidir.

Dersin İçeriği :

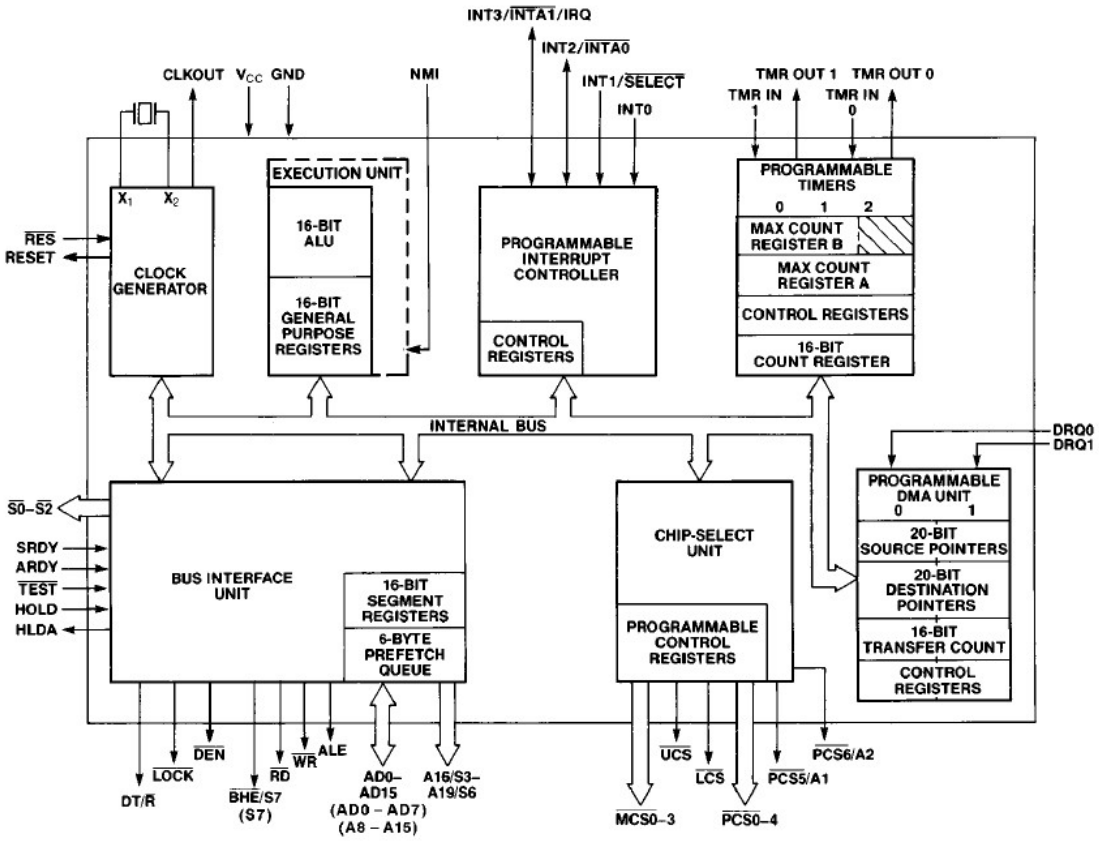
1. **Mikroişlemci Temelli Sistem Teknolojisi**
2. **80x86 Mimarisi**
3. **80x86 Mikroişlemci Donanımı**
4. **80x86 Merkezi İşlem Birimi Modülü Tasarımı**
5. **Ana Bellek Sisteminin Tasarımı ve Kesme Yapısı**
6. **80x86 Mikroişlemci Yazılımı**
7. **80x86 Mikroişlemci Komut Kümesi**
8. **Mikroişlemci Temelli Sistem Donanımı ve Yazılımı Geliştirme Sistemleri**
9. **Mikroişlemci Temelli Sistem Programlama Teknikleri**
10. **Temel Giriş/Çıkış Yöntemleri**
11. **80x86 Ailesi İçin Çevre Birimleri**
12. **80x86 Temelli Sistem Uygulamaları**
13. **IBM Uyumlu Kişisel Bilgisayar Sistem Donanımı ve Yazılımı**

Kaynaklar :

1. **The 80x86 Family Design, Programming, and Interfacing John UFFENBECK, Prentice-Hall, 1998**
2. **INTEL Microprocessors 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, Prentium ProProcessor, Pentium II, III, 4 , Barry B. Brey, Prentice-Hall, 2005**
3. **The 8086 Book, Russel RECTOR, George ALEXY, Osborne /McGraw-Hill, 1980**
4. **IBM PC/AT Assembly Language, Le SCANLON, Prentice-Hall, 1983**
5. **Microcomputers, Microprocessors : The 8080, 8085, Z80 Programming, Interfacing and Troubleshooting John UFFENBECK, Prentice-Hall, 1985**
6. **Intel Data Sheets**
7. **Mikroişlemciler ve Bilgisayarlar, Haluk GÜMÜŞKAYA, http://www.alfakitap.com/, 2002**
8. **http://www.yildiz.edu.tr/~uzun , http://www.tuncayuzun.com/**

80186/80188
HIGH-INTEGRATION 16-BIT MICROPROCESSORS

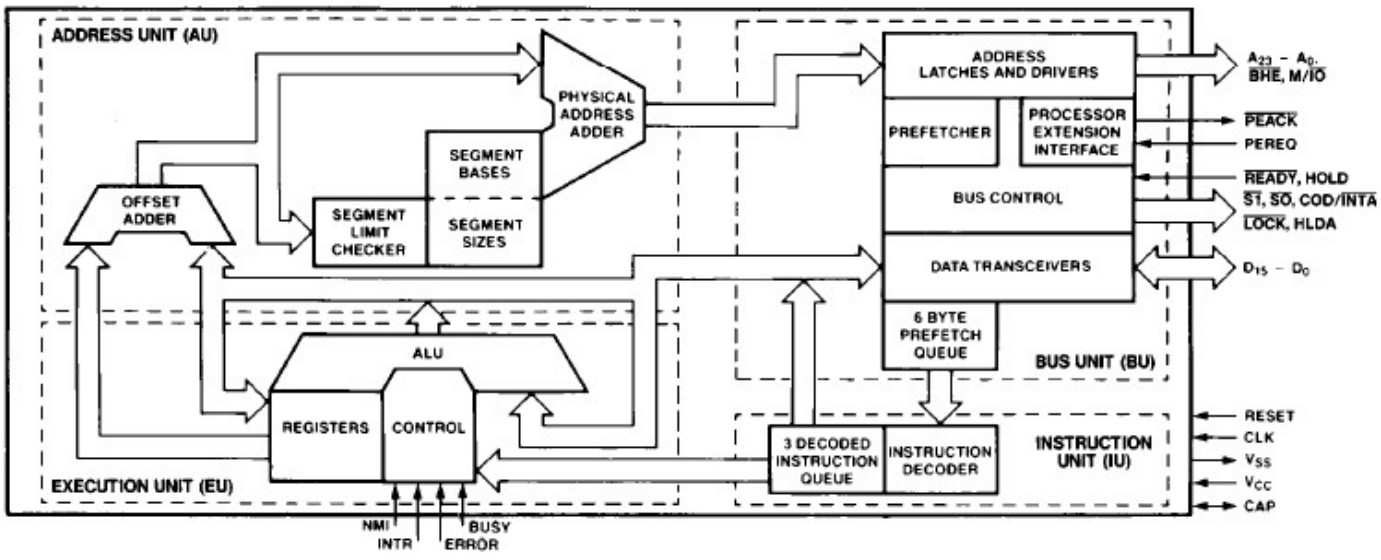
- Integrated Feature Set
  - Enhanced 8086-2 CPU
  - Clock Generator
  - 2 Independent DMA Channels
  - Programmable Interrupt Controller
  - 3 Programmable 16-bit Timers
  - Programmable Memory and Peripheral Chip-Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
- Available in 10 MHz and 8 MHz Versions
- High-Performance Processor
  - 4 Mbyte/Sec Bus Bandwidth Interface @ 8 MHz (80186)
  - 5 Mbyte/Sec Bus Bandwidth Interface @ 10 MHz (80186)
- Direct Addressing Capability to 1 Mbyte of Memory and 64 Kbyte I/O
- Completely Object Code Compatible with All Existing 8086, 8088 Software
  - 10 New Instruction Types
- Numerics Coprocessing Capability Through 8087 Interface
- Available in 68 Pin:
  - Plastic Leaded Chip Carrier (PLCC)
  - Ceramic Pin Grid Array (PGA)
  - Ceramic Leadless Chip Carrier (LCC)
- Available in EXPRESS
  - Standard Temperature with Burn-In
  - Extended Temperature Range (−40°C to +85°C)



80286
High Performance Microprocessor with Memory Management and Protection

(80286-12, 80286-10, 80286-8, 80286-6)

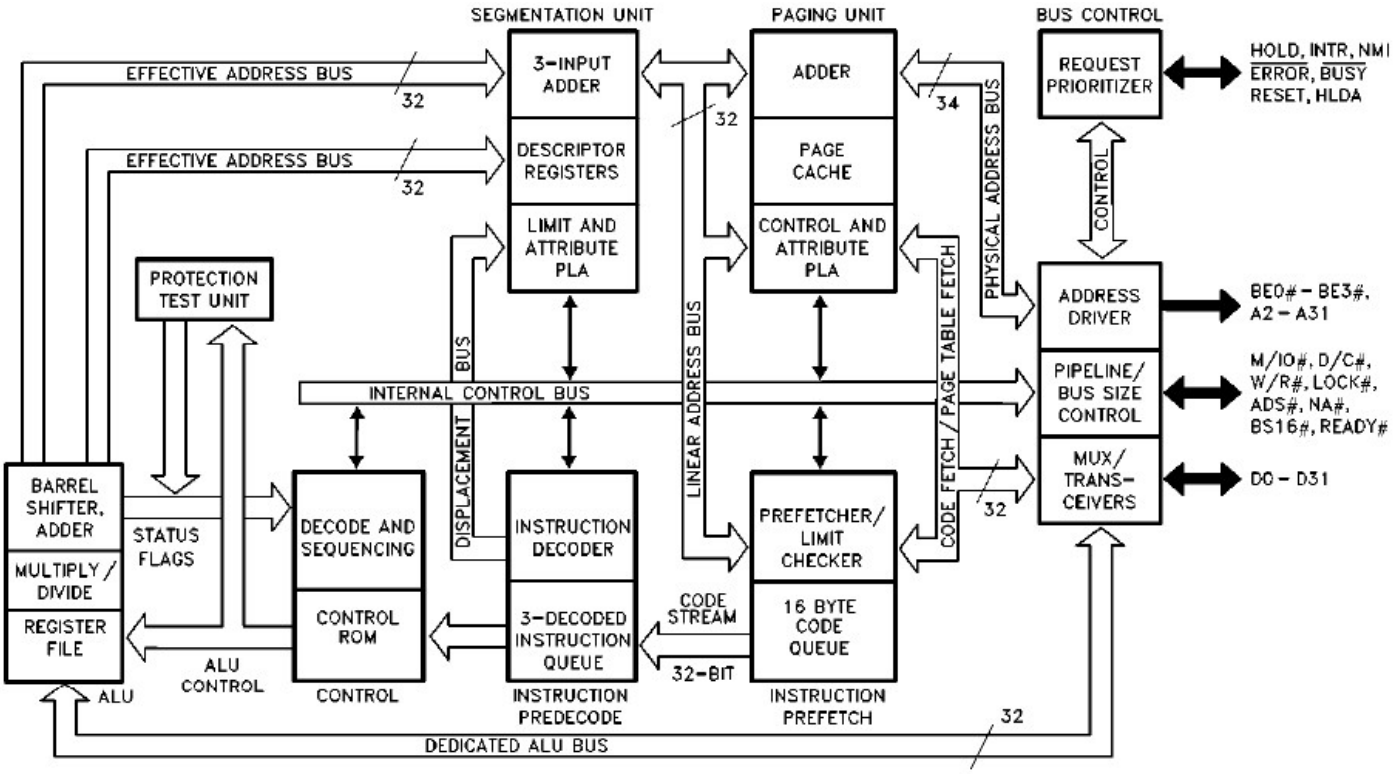
- High Performance Processor (Up to six times 8086)
- Large Address Space:
  - 16 Megabytes Physical
  - 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 8086 Upward Compatible Operating Modes:
  - 8086 Real Address Mode
  - Protected Virtual Address Mode
- Optional Processor Extension:
  - 80287 High Performance 80-bit Numeric Data Processor
- Range of clock rates
  - 12.5 MHz for 80286-12
  - 10 MHz for 80286-10
  - 8 MHz for 80826-8
  - 6 MHz for 80286-6
- Complete System Development Support:
  - Development Software: Assembler, PL/M, Pascal, FORTRAN, and System Utilities
  - In-Circuit-Emulator (ICE™-286)
- High Bandwidth Bus Interface (12.5 Megabyte/Sec)
- Available in 68 Pin Ceramic LCC (Leadless Chip Carrier) and PGA (Pin Grid Array) Packages



Intel386™ DX MICROPROCESSOR
32-BIT CHMOS MICROPROCESSOR
WITH INTEGRATED MEMORY MANAGEMENT

- Flexible 32-Bit Microprocessor
  - — 8, 16, 32-Bit Data Types
  - — 8 General Purpose 32-Bit Registers
- Very Large Address Space
  - — 4 Gigabyte Physical
  - — 64 Terabyte Virtual
  - — 4 Gigabyte Maximum Segment Size
- Integrated Memory Management Unit
  - — Virtual Memory Support
  - — Optional On-Chip Paging
  - — 4 Levels of Protection
  - — Fully Compatible with 80286
- Object Code Compatible with All 8086 Family Microprocessors
- Virtual 8086 Mode Allows Running of 8086 Software in a Protected and Paged System
- Hardware Debugging Support
- Optimized for System Performance
  - — Pipelined Instruction Execution
  - — On-Chip Address Translation Caches
  - — 20, 25 and 33 MHz Clock
  - — 40, 50 and 66 Megabytes/Sec Bus Bandwidth
- Numerics Support via Intel387™ DX Math Coprocessor
- Complete System Development Support
  - — Software: C, PL/M, Assembler System Generation Tools
  - — Debuggers: PSCOPE, ICE™-386
- High Speed CHMOS IV Technology
- 132 Pin Grid Array Package
- 132 Pin Plastic Quad Flat Package

  (See Packaging Specification, Order #231369)



Intel386™ DX Pipelined 32-Bit Microarchitecture

EMBEDDED WRITE-BACK ENHANCED IntelDX4™ PROCESSOR

- Up to 100 MHz Operation
- Integrated Floating-Point Unit
- Speed-Multiplying Technology
- 32-Bit RISC Technology Core
- 16-Kbyte Write-Back Cache
- 3.3 V Core Operation with 5 V Tolerant I/O Buffers
- Burst Bus Cycles
- Dynamic Bus Sizing for 8- and 16-bit Data Bus Devices
- SL Technology
- Data Bus Parity Generation and Checking
- Boundary Scan (JTAG)
- 3.3-Volt Processor, 75 MHz, 25 MHz CLK
  - — 208-Lead Shrink Quad Flat Pack (SQFP)
- 3.3-Volt Processor, 100 MHz, 33 MHz CLK
  - — 208-Lead Shrink Quad Flat Pack (SQFP)
  - — 168-Pin Pin Grid Array (PGA)
- Binary Compatible with Large Software Base

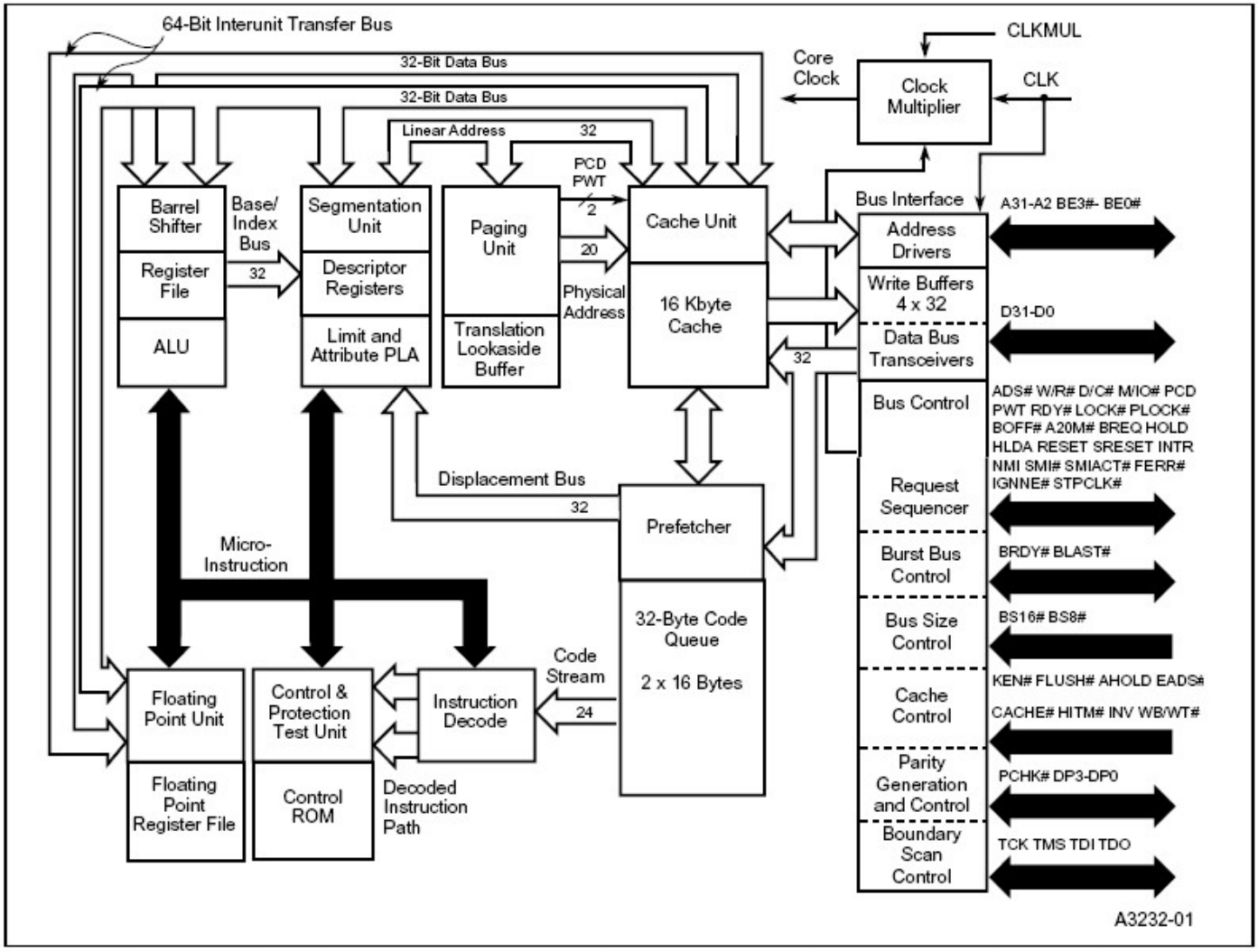
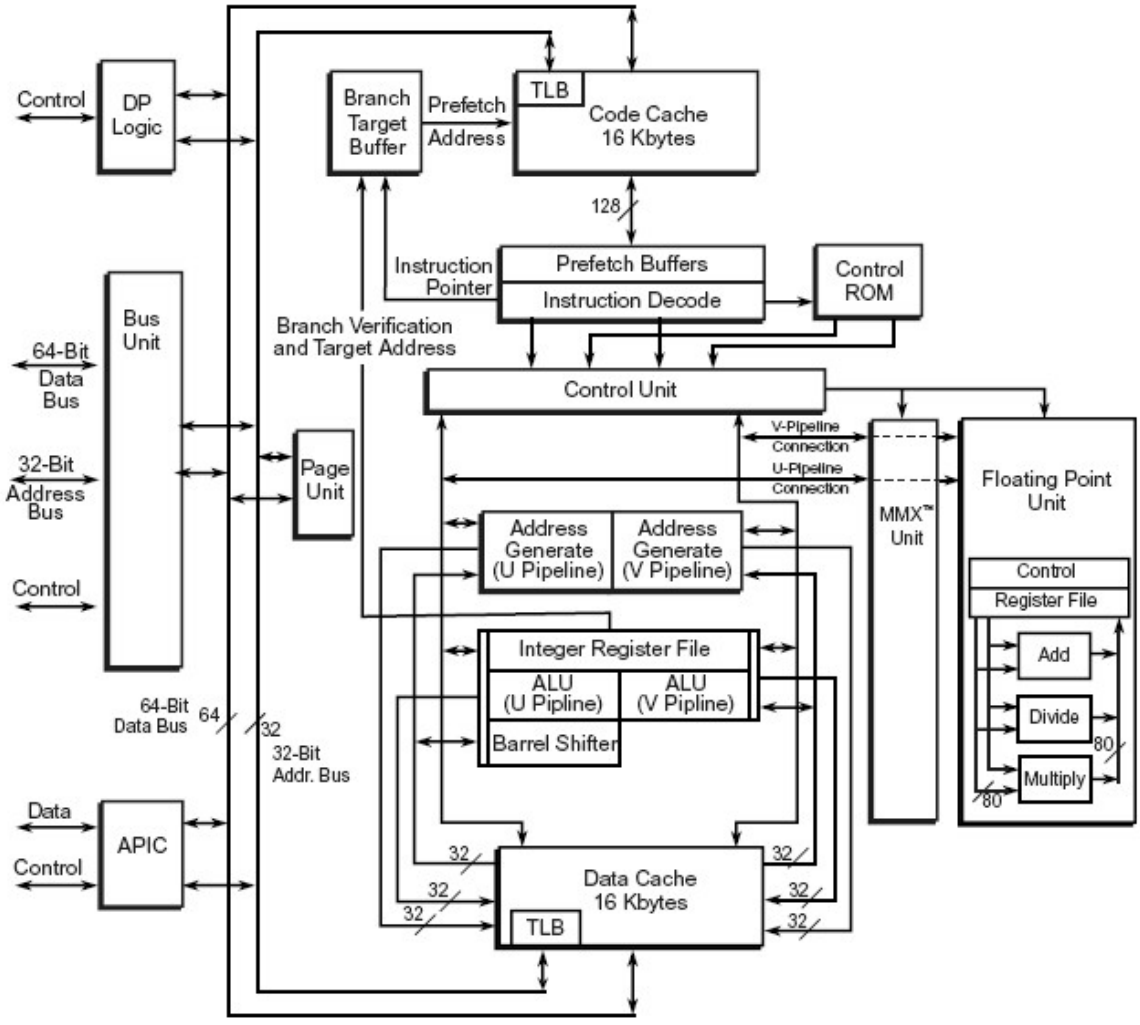


Figure 1. Embedded Write-Back Enhanced IntelDX4™ Processor Block Diagram

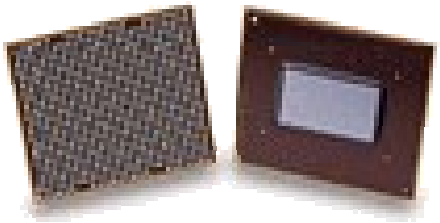
Embedded Pentium® Processor with MMX™ Technology

- Support for MMX™ Technology
- Compatible with Large Software Base
  - —MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit Processor with 64-Bit Data Bus
- Superscalar Architecture
  - —Enhanced Pipelines
  - —Two Pipelined Integer Units Capable of Two Instructions per Clock
  - —Pipelined MMX Technology Unit
  - —Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - —16-Kbyte Code, 16-Kbyte Write Back Data
  - —MESI Cache Protocol
- Advanced Design Features
  - —Deeper Write Buffers
  - —Enhanced Branch Prediction Feature
  - —Virtual Mode Extensions
- Enhanced CMOS Silicon Technology
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Dual Processing Configuration
- Internal Error Detection Features
- Multiprocessor Support
  - —Multiprocessor Instructions
  - —Support for Second Level Cache
- On-Chip Local APIC Controller
  - —Multiprocessor Interrupt Management
  - —8259 Compatible
- Power Management Features
  - —System Management Mode
  - —Clock Control
- Fractional Bus Operation
  - —233 MHz Core/66 MHz Bus (iCOMP® Index 2.0 rating=203)†
  - —200 MHz Core/66 MHz Bus (iCOMP® Index 2.0 rating=182)†
- Plastic Pin Grid Array Package



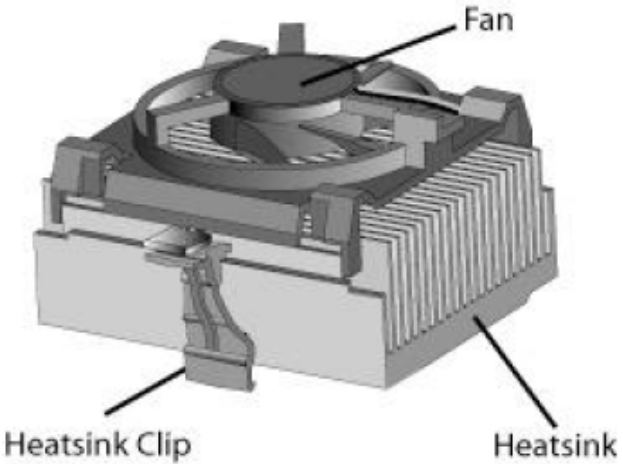
Pentium® II processors - Low Power

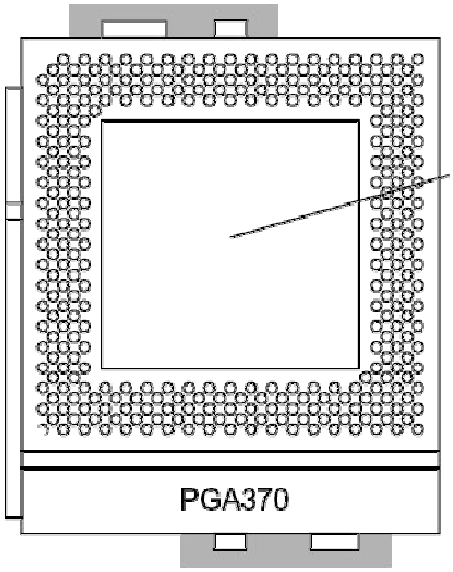
Product Number	Core Speed (MHz)	L2 Cache	External Bus Speed (MHz)	Thermal Design Power (Max)	Voltage	$T_{junction}$	Package
KC80524KX266256	266	256K	66	9.8W	1.6V	0-100C	615 BGA
KC80524KX333256	333	256K	66	11.8W	1.6V	0-100C	615 BGA

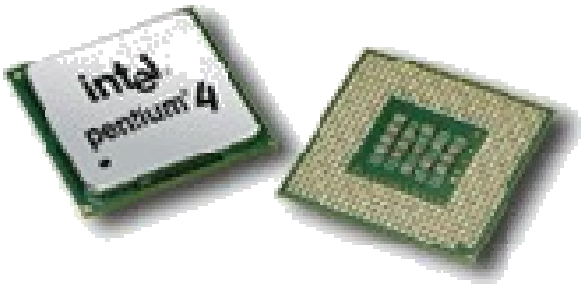


Pentium® III processors

Product Number	Core Speed (MHz)	L2 Cache	External Bus Speed (MHz)	Thermal Design Power (Max)	Voltage	$T_{junction}$	Package
RK80530KZ012512	1.26 GHz	512K	133	29.5W	1.45V	69C	370 FC-PGA2
RB80526PZ001256	1 GHz	256K	133	29.0W	1.75V	75C	370 FC-PGA
RB80526PY850256	850	256K	100	25.7W	1.75V	80C	370 FC-PGA
RB80526PZ733256	733	256K	133	22.8W	1.75V	80C	370 FC-PGA
RB80526PY700256	700	256K	100	21.9W	1.75V	80C	370 FC-PGA
RB80526PY600256	600	256K	100	19.6W	1.75V	82C	370 FC-PGA





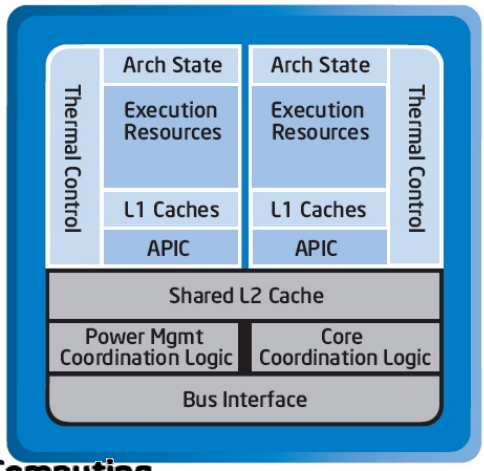


Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology[1]

Datasheet

2 GHz – 3.40 GHz Frequencies Supporting Hyper-Threading Technology[1] at 3.06 GHz with 533 MHz System Bus and All Frequencies with 800 MHz System Bus

- Available at 2 GHz, 2.20 GHz, 2.26 GHz, 2.40 GHz, 2.50 GHz, 2.53 GHz, 2.60 GHz, 2.66 GHz, 2.80 GHz, 3 GHz, 3.06 GHz, 3.20 GHz, and 3.40 GHz
- Supports Hyper-Threading Technology (HT Technology) at 3.06 GHz with 533 MHz system bus and all frequencies with 800 MHz system bus
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel NetBurst® microarchitecture
- System bus frequency at 400 MHz, 533 MHz, and 800 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper-Pipelined Technology
  - —Advance Dynamic Execution
  - —Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 8-KB Level 1 data cache
- Level 1 Execution Trace Cache stores 12-K micro-ops and removes decoder latency from main execution loops
- 512-KB Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 2-MB Integrated Level 3 (L3) cache with 8-way associativity that is supported by Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 478-Pin Package



Intel® Core™2 Duo Processors for Embedded Computing

Product Number	Core Speed	Front-Side Bus Speed	L2 Cache	Package
Intel® Core™2 Duo Processor E6400[Δ]				
HH80557PH0462M	2.13 GHz	1066 MHz	2 MB Unified	LGA775
Intel® Core™2 Duo Processor T7400[Δ]				
LE80537GF0484M	2.16 GHz	667 MHz	4 MB Unified	479 µFC-BGA
LF80537GF0484M	2.16 GHz	667 MHz	4 MB Unified	478 µFC-PGA

The Intel® Core™2 Duo mobile processor for Intel® Centrino® Duo mobile technology based on the Intel 945 Express Chipset family is built on 65-nanometer process technology and is the next generation high-performance, low-power mobile processor based on the Intel® Core™ architecture.

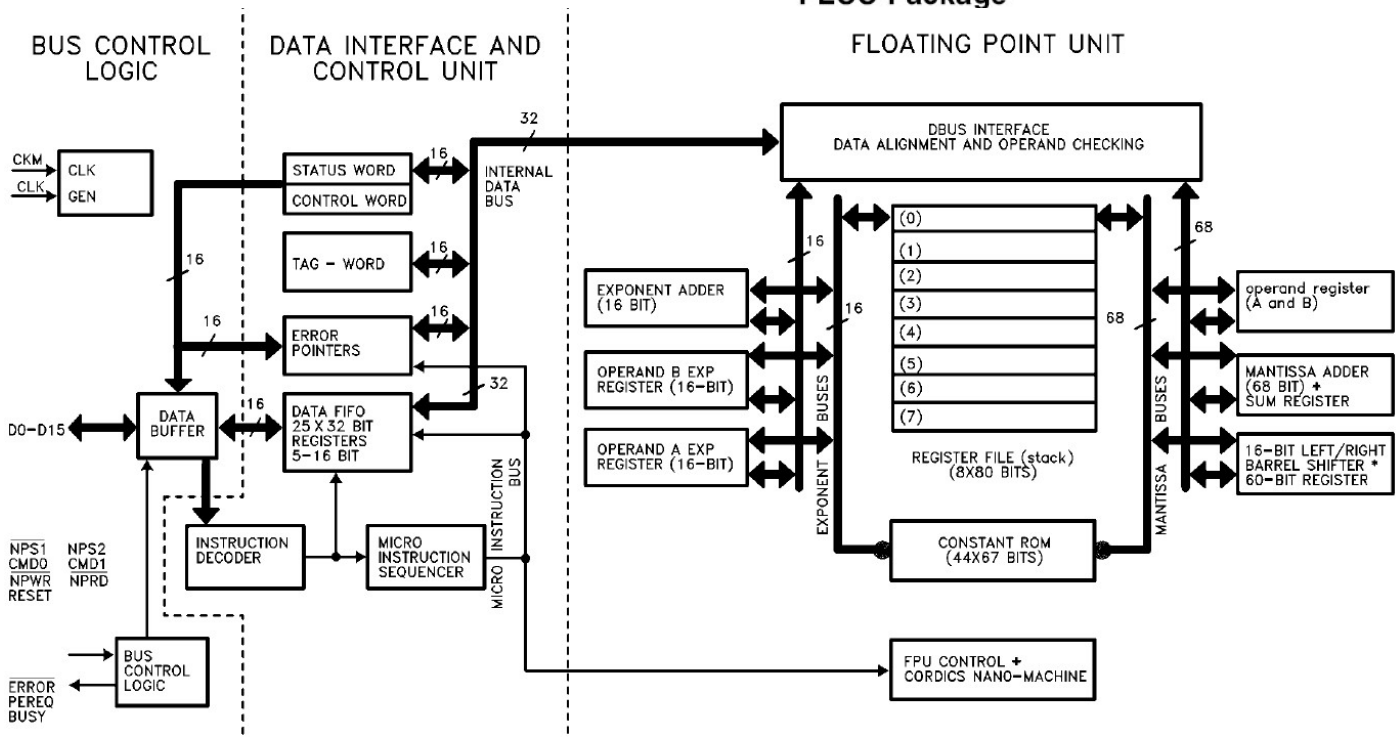
All references to the word "processor" in this document are references to the Intel Core 2 Duo mobile processor with 533- and 667-MHz Front Side Bus (FSB), unless specified otherwise.

The following list provides some of the key features on this processor:

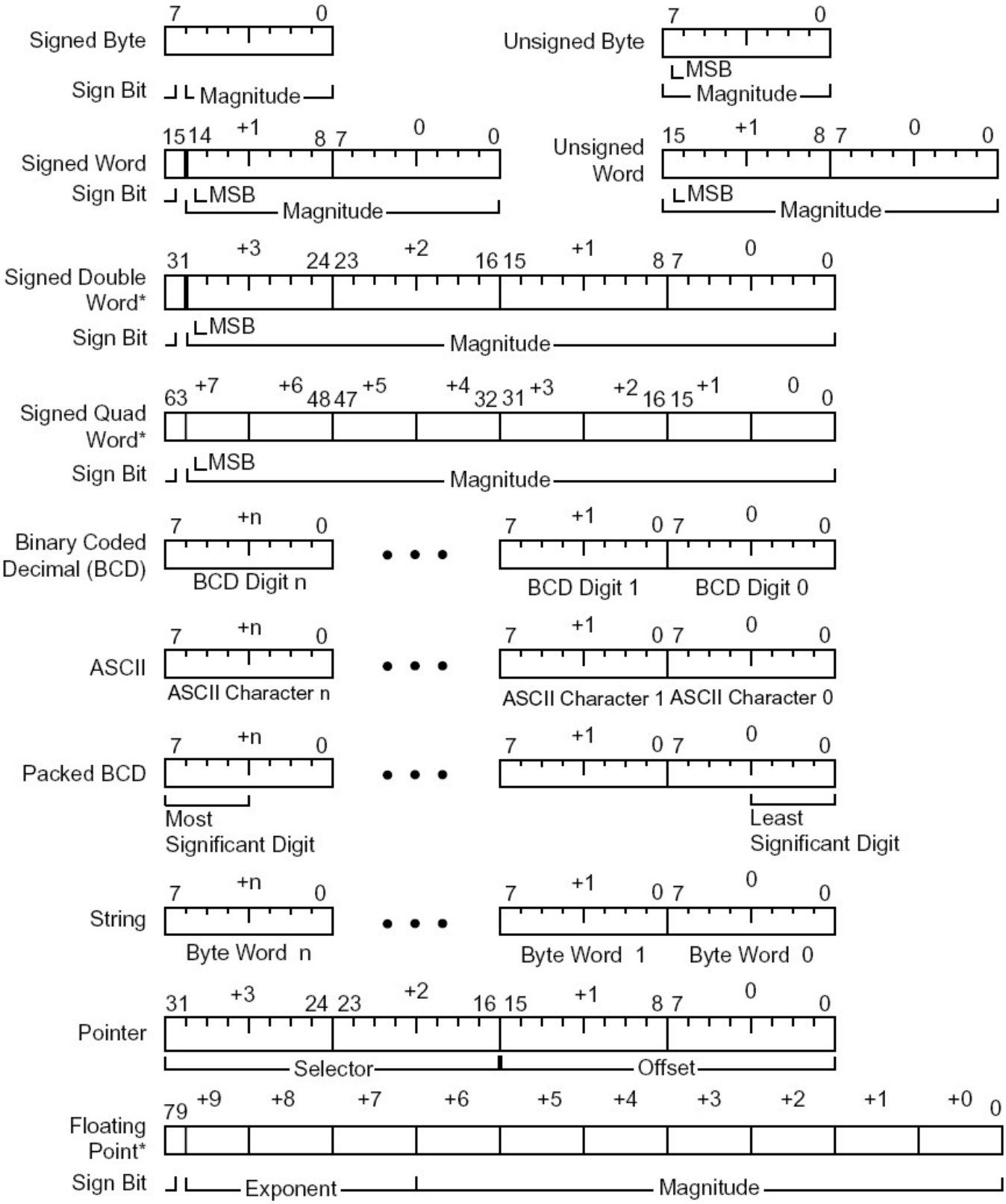
- Dual core processor for mobile with enhanced performance
- Intel® 64 architecture
- Supports Intel Architecture with Dynamic Execution
- On-die, primary 32-kB instruction cache and 32-kB write-back data cache per core
- On-die, up to 4-MB second level shared cache with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3)
- 667-MHz, Source-Synchronous FSB for Standard Voltage processors
- Advanced Power Management features including Enhanced Intel SpeedStep® Technology
- Intel® Enhanced Deeper Sleep state and Dynamic Cache Sizing
- Digital Thermal Sensor
- Micro-FCPGA and Micro-FCBGA packaging technologies
- Intel® Virtualization Technology
- Execute Disable Bit support for enhanced security

80C187
80-BIT MATH COPROCESSOR

- High Performance 80-Bit Internal Architecture
- Implements ANSI/IEEE Standard 754-1985 for Binary Floating-Point Arithmetic
- Upward Object-Code Compatible from 8087
- Fully Compatible with 387DX and 387SX Math Coprocessors. Implements all 387 Architectural Enhancements over 8087
- Directly Interfaces with 80C186 CPU
- 80C186/80C187 Provide a Software/ Binary Compatible Upgrade from 80186/82188/8087 Systems
- Expands 80C186's Data Types to Include 32-, 64-, 80-Bit Floating-Point, 32-, 64-Bit Integers and 18-Digit BCD Operands
- Directly Extends 80C186's Instruction Set to Trigonometric, Logarithmic, Exponential, and Arithmetic Instructions for All Data Types
- Full-Range Transcendental Operations for SINE, COSINE, TANGENT, ARCTANGENT, and LOGARITHM
- Built-In Exception Handling
- Eight 80-Bit Numeric Registers, Usable as Individually Addressable General Registers or as a Register Stack
- Available in 40-Pin CERDIP and 44-Pin PLCC Package

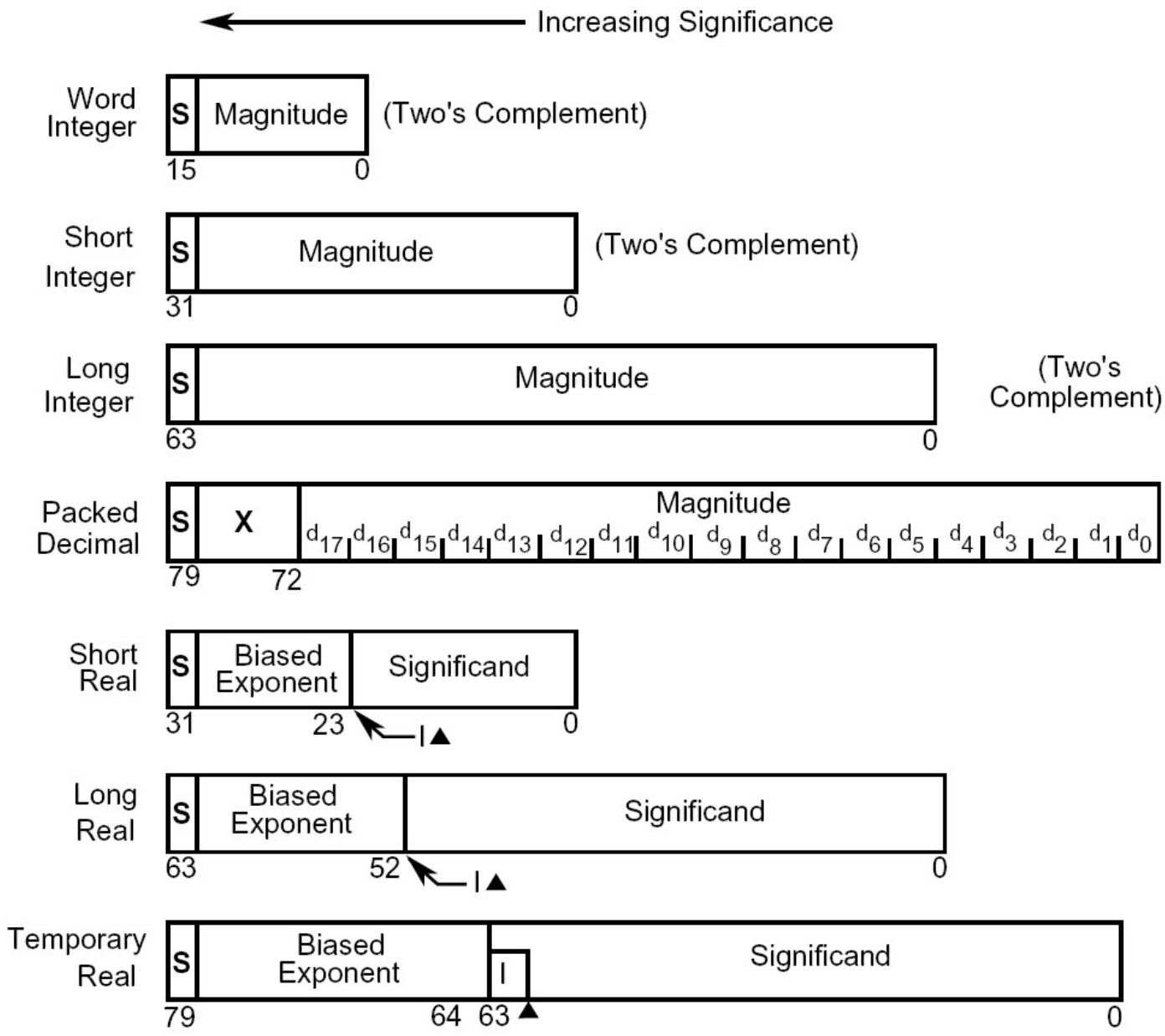


80C186 VERİ TİPLERİ



NOTE: *Directly supported if the system contains an 80C187.

80C187 VERİ TİPLERİ



NOTES:

S = Sign bit (0 = positive, 1 = negative)

d_n = Decimal digit (two per byte)

X = Bits have no significance; 80C187 ignores when loading, zeros when storing.

▲ = Position of implicit binary point

I = Integer bit of significand; stored in temporary real, implicit in short and long real

Exponent Bias (normalized values):

Short Real: 127 (7FH)

Long Real: 1023 (3FFH)

Temporary Real: 16383 (FFFH)

80C187-Supported Data Types

Intel387™ DX
MATH COPROCESSOR

- High Performance 80-Bit Internal Architecture
- Implements ANSI/IEEE Standard 754-1985 for Binary Floating-Point Arithmetic
- Expands Intel386™ DX CPU Data Types to Include 32-, 64-, 80-Bit Floating Point, 32-, 64-Bit Integers and 18-Digit BCD Operands
- Directly Extends Intel386™ DX CPU Instruction Set to Include Trigonometric, Logarithmic, Exponential and Arithmetic Instructions for All Data Types
- Upward Object-Code Compatible from 8087 and 80287
- Full-Range Transcendental Operations for SINE, COSINE, TANGENT, ARCTANGENT and LOGARITHM
- Built-In Exception Handling
- Operates Independently of Real, Protected and Virtual-8086 Modes of the Intel386™ DX Microprocessor
- Eight 80-Bit Numeric Registers, Usable as Individually Addressable General Registers or as a Register Stack
- Available in 68-Pin PGA Package
- One Version Supports 16 MHz–33 MHz Speeds